Sintering temperature, microstructure and resistivity of polycrystalline $Sm_{0.2}Ce_{0.8}O_{1.9}$ **as SOFC's electrolyte**

GUOR-BING JUNG, TA-JEN HUANG∗ *Department of Chemical Engineering, National Tsing-Hua University, Hsinchu, Taiwan, Republic of China E-mail: tjhuang@che.nthu.edu.tw*

In this work, near-completely soft-agglomerated $Sm_{0.2}Ce_{0.8}O_{1.9}$ powders have been prepared. The pellets were formed and sintered at various sintering conditions of temperature and time. It was found that the sintering conditions have significant effects on the pellet resistivity. By the measurements with the DC four-probe method, it was found that the overall resistivity of the polycrystalline $Sm_{0.2}Ce_{0.8}O_{1.9}$ material sintered at 1500°C increases linearly with the reciprocal of the average grain size. The AC impedance spectroscopy has been used to distinguish the grain resistivity and the apparent grain boundary resistivity. The "brick layer" microstructural model has been used to provide an estimate of the apparent grain boundary resistivity and to relate the electrical properties to the microstructural parameters. By lowering the sintering temperature to 1100–1200◦C, the true grain boundary resistivity was nearly two orders lower than that sintered at 1500◦C, and thus the overall resistivity decreases to about 31 ohm-cm at 700◦C measurement. This makes the $Sm_{0.2}Ce_{0.8}O_{1.9}$ material capable of working as SOFC's electrolyte at temperatures lower than 700◦C. ^C *2003 Kluwer Academic Publishers*

1. Introduction

Solid electrolytes with high oxygen vacancy conductivity are of special interest for application in electrochemical devices such as solid oxide fuel cell (SOFC), sensors, oxygen separation system, syngas production, etc. In the case of SOFC, operation at as low temperature as possible is desirable from the standpoint of choice of inexpensive metallic materials for interconnects and system reliability. A typical operating temperature for the state-of-the-art zirconia-based SOFC is 1000◦C, although thin film approaches on laboratory scales have been successful in lowering the cell operation temperature below 800◦C.

Operation below 700◦C may require electrolytes with lower resistivity than yttria-stabilized zirconia (YSZ). There are several potential candidates such as ceria-based materials and perovskites. Research is underway at several laboratories on ceria-based electrolytes because they exhibit lower ionic resistivity at a given temperature compared to the YSZ electrolytes [1–5]. However, the use of such electrolytes in SOFC has been excluded for many years as it is well known that ceria becomes a mixed conductor in reducing atmospheres due to the formation of the electronic charge carriers associated with the partial reduction of ceria. The electronic charge carriers formed would then short-circuit the cell. It has been reported that the reduction for ceria-based materials can be neglected at lower temperature as 600° C–700 $^{\circ}$ C [6]. However, such low temperature is not suitable for ceria operation as SOFC's electrolyte due to high resistivity of the material.

For a given material such as ceria, resistivity can be minimized by a judicious selection of aliovalent cation and its concentration. However, in addition to the dopant type and concentration, oxygen vacancy resistivity of polycrystalline ceria also depends strongly on fabrication parameters, such as the sintering temperature [6, 7], since this often dictates the grain size and the nature of the grain boundary, such as resistivity, which is generally 100 to 1000 times larger than that of the grain after annealing. This results from the segregation of solute (e.g., Y'_{Zr}) at space charge layer near grain boundary which will increase the probability of the formation of $(Y_{Zr}V_{o}^{..})$, thus the association enthalpy is increased and the activation energy of the grain boundary resistivity is higher. After quenching from high temperature, the grain boundary resistivity is quite small due to insufficient time for the segregation of solute Y'_{Zr} to the grain boundary to form $(Y_{Zr}V_{o}^{..})$, and thus the activation energy is lower.

At the sintering temperatures higher than 1450° C, the decrease in resistivity due to the grain boundary effect can be interpreted in terms of a space charge layer, which will impede the oxygen vacancy transport. Therefore, the grain boundary contribution to resistivity often increases with the decrease of the grain size; this has been verified with polycrystalline ceria doped with various rare-earth oxides $(Y_2O_3, Dy_2O_3, Er_2O_3,$ Gd_2O_3 , Yb_2O_3 [6, 8, 9].

In this work, the relationship between the overall resistivity of the polycrystalline $Sm_{0.2}Ce_{0.8}O_{1.9}$ material and the grain size was studied by the DC four-probe method, and also investigated via the AC impedance spectroscopy. The effect of the sintering temperature and time on the resistivities was studied and the observed phenomena were explained with the grain boundary effect.

In addition, in this work, by going to a lower sintering temperature of 1100–1200◦C, we observed a lower overall resistivity of 31 ohm-cm at 700◦C measurement which should enable the operation temperature of the ceria-based electrolytes be further decreased to 600-plus◦C from 800◦C.

2. Experiment details

2.1. Sample preparation

The sample $\rm Sm_0$ $_2$ Ce_{0.8}O_{1.9} was prepared from reagentgrade (99% purity, Aldrich Chemical Co.) metal nitrates $Sm(NO₃)₃ · 6H₂O$ and $Ce(NO₃)₃ · 6H₂O$. The appropriate proportions of samarium nitrate and cerium nitrate were dissolved in distilled water to make 0.1– 0.2 M solutions. Hydrolysis of the metal salts to hydroxides was obtained by dropping into NH4OH solution. To eliminate the inhomogeneous gels, nitrate solutions were added dropwise to a 4 N solution of NH4OH and the solution was maintained at $pH > 9$. A distinct deeply purple color of precipitate gel was formed when the nitrate solution was dropped into the NH4OH solution. The gel was easily isolated by vacuum filtration. The recovered gel was immersed in octanol and boiled on a hot plate. During boiling the gel shrunk substantially and the color changed from purple to black.

The gel was dried at 130◦C in a tubular drier overnight to remove the solvent. After heating at 600◦C for two hours, the powder with soft-agglomerates was pressed and sintered at temperatures ranging from 1000 to 1500◦C for different time. In order to get theoretical density higher than 94%, the pellet should be sintered for 5 hrs at temperature higher than 1300◦C, or for 20 hrs at 1100–1200◦C. It is observed that only 85% theoretical density could be obtained for sample sintered for 20 hrs at 1000◦C. The density test was conducted by the Archimedes method, as described in our previous study [10].

2.2. Microstructural analysis

The microstructure was analyzed with Scanning Electron Microscopy (SEM, JEOL JSM-5600) and the bulk density of the sintered samples was determined by the Archimedes method using distilled water.

2.3. Electrical measurements

The samples of the sintered pellets with 0.9–1.5 mm thick were sanded to keep surface smooth. Both

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DC-four probe and AC impedance spectroscopy have been used in this study. As for AC impedance spectroscopy measurement, Pt paste was painted on both sides of the pellets with area of $0.9-1.5$ mm² as electrodes. The samples with Pt wires attached to the electrodes were fired at 1000◦C for one hour to ensure good bond between the sample surface and the Pt electrode and also to burn off the solvent in the paste. The impedance spectroscopy technique has been used in order to distinguish the relative contributions to the total ionic resistivity, which comes from both the grain interior and the grain boundary. Measurement was made every 50◦C ranging from 400 to 900◦C. An electrochemical analyzer (CH Instruments, chi604a) was used. The frequency range analyzed was from 0.001 to 100 kHz and the amplitude was 40 mV.

At low temperatures three arcs can normally be resolved in complex impedance spectra obtained from the polycrystalline oxygen-vacancy conducting electrolytes. These correspond, in order of increasing frequency, to polarization of electrode, grain boundary, and grain interior, respectively. Also note that an idealized equivalent circuit, as first reported by Bauerle [11], is most often used to represent the electrical behavior of the polycrystalline oxygen-vacancy conducting electrolytes.

3. Results and discussion

3.1. Effect of microstructural properties on resistivity

In this work, near-completely soft-agglomerated [10] $\text{Sm}_{0.2}\text{Ce}_{0.8}\text{O}_{1.9}$ powders have been prepared. The softagglomerated powders can yield 94% relative density by sintering at 1200◦C for 20 hrs.

Figs 1 and 2 show two series of SEM photographs which were all taken with the same magnification $(\times 20000)$ and depict typical areas of the microstructure of each of the sample used in the electrical measurements. As shown in Fig. 1, there is little grain growth for pellet sintering at temperatures ranging from 1100 to 1400◦C. However, when the sintering temperature is raised from 1400 to 1500◦C, there is a significant grain growth, as shown in Fig. 2. This agrees with the results of the cation transport being the rate-limiting step for grain growth [12]. Note that the cations are less mobile until a temperature around 1450◦C.

Fig. 3 show the polycrystalline overall resistivity (ρ) as a function of inverse average grain size $(\frac{1}{d})$ for $Sm_{0.2}Ce_{0.8}O_{1.9}$ sintered at 1500°C. It is seen that the relationships of ρ vs. $\frac{1}{q}$ can be adequately represented by straight lines and the slope decreases with the increase of the temperature of conductivity measurement. The regression coefficients of the fitting straight lines were all higher than 0.99. As shown by the 600◦C line in Fig. 3, the conductivity increases (or resistivity decreases) by a factor of about 2 when the grain size (*d*) increases about two times from 0.67 to 1.33 μ m.

Grain size dependence of resistivity can be described in term of the "brick layer" model [13]. In this model, the material is assumed to consist of an array of cubic shaped grains with edges of length *d*, separated by flat grain boundary of thickness of δ_{gb} where $d \gg \delta_{gb}$.

Figure 1 Series of SEM photographs for samples with various sintering temperatures: (a) 1100°C, (b) 1200°C, (c) 1300°C, and (d) 1400°C.

Current flow is assumed to be one dimension and curvature of the current path at the corn of the grain is neglected. It is also assumed that the grain boundary has greater resistance to oxygen vacancy transport compared to the grain interior. Thus, the polycrystalline resistivity can be simply given as a sum of resistance to transport through grains and across the grain boundaries. In terms of the microstructural parameters such as the grain size (*d*) and the grain boundary thickness (δ) , the overall resistivity is given by

$$
\rho = \rho_{g} + \frac{\lambda \delta_{gb}}{d} \rho_{gb}^{*} \tag{1}
$$

where ρ , ρ_g , λ , ρ_{gb}^* , and $\frac{\delta}{d} \rho_{gb}^*$ are, respectively, overall resistivity, grain resistivity, dimensionless geometrical factor, true grain boundary resistivity, and apparent grain boundary resistivity (defined as ρ_{gb}). Such an equation was originally used to describe the relationship between resistivity and microstructure in β'' alumina [14, 15] and was applied recently to describe the resistivity with microstructure of rare-earth oxidedoped ceria [6].

Equation 1 implies that the intercept of ρ vs. $\frac{1}{d}$ line is the grain resistivity (ρ_g) with the proportionality constant being $\lambda \delta_{\text{gb}} \rho_{\text{gb}}^*$. The dimensionless geometric factor (λ) can be evaluated based on the knowledge of microstructure. However, the grain boundary thickness (δ_{gb}) can not be easily measured nor calculated theoretically. The reason is that the actual δ_{gb} may not have any relation with the physically distinct grain boundary region. Fortunately, it can be reasonable expected that at the temperature of conductivity measurement, δ_{gb} will be constant. Thus, temperature dependence of the slope can be clearly attributed to the temperature dependence of ρ_{gb}^* , assuming that λ is essentially independent of grain size, an assumption that should be valid as long as the grain shape does not change with size and this has been proven in the above microstructural analysis.

3.2. Effect of sintering conditions on resistivity

3.2.1. Sintering time

Fig. 4 shows the actual complex impedance data obtained for the samples at measurement temperature of 400 \degree C. At 400 \degree C, only the grain interior arcs can be seen to have been well resolved in the impedance spectrum, the start of the grain boundary arc is also presented and is clearly overlapping the electrode arc. It can also be seen that as the sintering time increased, there was a small reduction of the resistance that is associated with the grain boundary.

Figure 2 Series of SEM photographs for samples sintered at 1500°C with various time: (a) 1 hr, (b) 5 hr, (c) 8 hr, and (d) 11 hr.

Figure 3 Overall resistivity vs. inverse grain size at various measurement temperatures: (\bullet) 600°C, (\circ) 650°C, ($+$) 700°C, (\Box) 800°C, (\blacktriangle) 000°C 900°C.

At measurement temperatures higher than 600◦C, only arcs of grain boundary can be completely resolved and there was almost no sign of the grain interior arc due to the limitation in the high frequency of our machine. However, in order to get useful information from the complex impedance spectra, the resistance of both grain

Figure 4 Complex impedance data obtained at 400◦C for samples sintered at 1500°C with various time: (Δ) 2 hr, (\bullet) 4 hr, (\Box) 5 hr.

Figure 5 Apparent grain boundary resistivity for samples with various sintering time: (○) 2 hr, (▲) 3 hr, (▲) 4 hr, (□) 5 hr, (●) 11 hr. With measurement temperature of 600, 700, 800, 900◦C, respectively.

 (R_g) and the grain boundary (R_{gb}) should be converted to electrical resistivity (ρ') simply by consideration of sample geometry in the usual manner as Equation 2.

$$
\rho' = \frac{R}{\left(\frac{t}{a}\right)}\tag{2}
$$

where *t* is the sample thickness and *a* is the Pt electrode area.

The calculated results for samples sintered at 1500◦C with various time are shown in Fig. 5, with measurement temperature of 600, 700, 800, 900◦C, respectively. As shown by these results, the grain resistivity (ρ_g) changes little regardless of the variation of the sintering time. Fig. 5 also shows a comparison of $\rho_{\rm g}$ with the data from the DC four-probe measurements. It is seen that there is good agreement between these two kinds of measurements.

The above observation of little change of grain resistivity with sintering time is similar to the result of Dijk [15]. However, the apparent grain boundary resistivity decreases with increasing sintering time. This means that the apparent grain boundary resistivity decreases with the increase of the grain size as shown in Fig. 2. In addition, it is found that the apparent grain boundary resistivity was nearly one order higher than the grain resistivity especially at low measurement temperature.

3.2.2. Sintering temperature

Fig. 6 shows the overall resistivity of polycrystalline $Sm_{0.2}Ce_{0.8}O_{1.9}$ sintered at various temperatures. It is

Figure 6 Overall resistivity vs. sintering temperature at various measurement temperatures: (\bullet) 600°C, (\blacktriangle) 650°C, (\blacksquare) 700°C, (\bigcirc) 800°C, (\land) 900°C, 31(DC) denotes the value of grain resistivity from the DC (Δ) 900°C; 31(DC) denotes the value of grain resistivity from the DC measurement at 700◦C.

seen that the overall resistivity decreases with lower sintering temperature especially at low measurement temperature, and attains a minimum at the sintering temperature of 1100–1200◦C. This minimum resistivity is about the same as the grain resistivity (ρ_g) from the DC measurement, e.g., 31 ohm-cm at 700◦C. This low resistivity makes the electrolyte material capable of working at 600-plus◦C, which requires a resistivity lower than 33 ohm-cm [16]. However, the overall resistivity increases as the sintering temperature is lowered further to 1000◦C. This may be due to increased porosity, which prevents direct grain contact and thus

Figure 7 Grain resistivity at 700℃ for samples with various sintering temperatures: (●) 1100°C, (▲) 1200°C, (○) 1300°C, (△) 1400°C, (■)
1500°C $1500°C$

leads to higher resistivity for oxygen vacancy transport [17].

As Fig. 7 shows, little change of grain resistivity occurs due to the variation of the sintering temperature. Therefore, in order to further explain the relationship of the measured electrical properties with the microstructural properties of samples sintered at various temperatures, it is convenient to define a microstructural model. A survey of ceramic microstructural models and associated electrical behavior is provided in [18]. When considering doped zirconia or doped ceria, the most widely adopted model has been the brick layer model, as described above.

Using the brick layer model one can describe two different situations depending on the relative magnitudes of the grain resistivity (ρ_g) and apparent grain boundary resistivity (ρ_{gb}). When $\rho_{gb} \gg \rho_{g}$, the current path will be predominantly through grain and across grain boundaries; when the reverse is true, the current path will be predominantly along grain boundaries. The former situation is more realistic for doped ceria or zirconia and this is confirmed in Fig. 5. For the situation that the grain boundary is more resistive than the grain, it is possible to derive the following expression relating the experimentally obtained electrical properties, i.e., apparent grain boundary resistivity (ρ_{gb}) , grain boundary capacitance (C_{gb}) and grain capacitance (C_g) , to the microstructural properties, i.e., δ_{gb} and *d*. According to the brick layer model, there are two basic equations

$$
C_{\rm gb}\frac{t}{a} = \varepsilon_{\rm o}\varepsilon_{\rm gb}\frac{d}{\delta_{\rm gb}}\tag{3}
$$

$$
C_g \frac{t}{a} = \varepsilon_0 \varepsilon_g \tag{4}
$$

where $\varepsilon_{\rm g}$ and $\varepsilon_{\rm gb}$ are the relative dielectric permittivity of grain and grain boundary, respectively. Dividing Equation 3 by Equation 4 and assuming that $\varepsilon_{\rm g} = \varepsilon_{\rm gb}$, we have

$$
\frac{C_{gb}}{C_g} = \frac{d}{\delta_{gb}}\tag{5}
$$

In addition, one needs to include grain boundary layer thickness (δ_{gb}) and grain size (*d*) to calculate the true grain boundary resistivity ρ_{gb}^* , defined as

$$
\rho_{gb}^* \equiv \rho_{gb} \frac{d}{\delta_{gb}} = R_{gb} \frac{a}{t} \frac{C_{gb}}{C_g} = \frac{R_{gb} C_{gb}}{C_g \frac{t}{a}} \tag{6}
$$

Assuming that $C_g \frac{t}{a}$ in Equation 4 is constant and equal to 1.8 nF, Equation 6 becomes

$$
\rho_{\text{gb}}^* = \frac{R_{\text{gb}} C_{\text{gb}}}{1.8 \times 10^{-9}} = \frac{10^9}{1.8 \,\omega} \tag{7}
$$

where ω is the frequency, which can be obtained from the impedance spectroscopy. The calculated data at different measurement temperatures are shown in Fig. 8, with the true grain boundary resistivity (ρ_{gb}^*) in log scale. It is seen that, as the sintering temperature increases from 1100 to 1200 \degree C, there is almost no change of ρ_{gb}^* , and only gradual change occurs as the sintering temperature further increases to 1300◦C. However, as the sintering temperature increases to $1500\degree C$, there is a dramatic increase of ρ_{gb}^* with about two orders. As the true grain boundary resistivity (ρ_{gb}^*) decreases by two orders, the second term at the right-hand side of Equation 1 becomes very small and thus the overall resistivity approximates to the grain resistivity. This explains the nearly one time decrease of the overall electrical resistivity as the sintering temperature decreasing from 1500 to $1100\degree$ C as shown in Fig. 6.

Fig. 9 shows the Arrhenius plot of the true grain boundary resistivity of $\text{Sm}_{0.2}\text{Ce}_{0.8}\text{O}_{1.9}$ sintered at various temperatures. From the Arrhenius equation,

$$
\frac{1}{\rho} = \left(\frac{A}{T}\right) \exp\left(\frac{-E_a}{kT}\right) \tag{8}
$$

the value of E_a is calculated from the slope of the straight line of Fig. 9. It is seen that the activation energy (*E*a) decreases from 2.84 eV for sample sintered at 1500◦C to 2.24 eV at 1100◦C. Note that these activation energies are much higher than that of 0.69 eV for the

Figure 8 True grain boundary resistivity vs. sintering temperature at various measurement temperatures: (■) 600°C, (▲) 650°C, (□) 700°C, (\bullet) 800°C, (\circ) 900°C.

Figure 9 Arrhenius plot of true grain boundary resistivity for samples with various sintering temperatures: (\triangle) 1100°C, (\triangle) 1200°C, (\blacksquare) 1300°C, (\circ) 1400°C, (\bullet) 1500°C. (\diamond): of grain resistivity.

grain interior, which is obtained from the variation of the grain resistivity as calculated via Equation 1 from the data shown on Fig. 3 and the Arrhenius equation.

From Fig. 9 and the Arrhenius Equation 8, it is seen that the average Arrhenius coefficient (*A*) changes from 23.0 for the grain boundary to 11.7 for the grain interior; this means that the number of oxygen vacancies at the grain boundary is nearly double that in the grain. It is also seen from Fig. 9 that the oxygen vacancy transports across the grain boundary with lower activation energy for sample sintered at lower temperature.

3.2.3. Space charge layer near grain boundary

Since most of the grain boundaries in this study might be precipitate-free, we could discuss in the following what contributes to the true grain boundary resistivity. In particular, we will examine the resistive contribution from the space charge layers near the grain boundaries.

The existence of the space charge layer near the lattice discontinuities in an ionic solid was first proposed by Frenkel [13]. The grain boundaries have been assumed to act as infinite sources and sinks for vacancies. According to Guo [19], the grain boundary resistance consists of the contribution from the grain boundary and the space charge layer. At thermodynamic equilibrium the grain boundary may carry an electric potential resulting from the presence of excess ions of one sign; this potential is compensated by a space charge potential of the opposite sign adjacent to the boundary. The nature of the space charge is dependent on the formation energy of the point defects in pure ionic crystals. It is likely, as in most practical cases, that the nature of the space charge is dictated by the effective charge of the aliovalent dopant [20, 21]. The electrical potential at the grain boundary will result in solute segregation in the space charge layer.

For the samples in this study, i.e., Sm_0 ₂Ce_{0.8}O_{1.9} pellets, it is proposed that the effectively positively charged oxygen vacancies (V_0^{\cdot}) are the predominate defects at the grain boundary. These vacancies are produced from the defect reaction as follows:

$$
2\mathrm{SmO}_{1.5} \to 2\mathrm{Sm}'_{\mathrm{Ce}} + V_{\mathrm{o}}^{\cdot\cdot} + 3\mathrm{O}_{\mathrm{O}}^{X} \tag{9}
$$

Therefore, the grain boundary will have a positive potential because of excess oxygen vacancies and this has been experimental proven by Tian and Chan [22] with $Y_{x}Ce_{1-x}O_{2-X/2}$. In order to maintain long-range charge neutrality, the negatively charged Sm'_{Ce} segregates to form the space charge layer. The formation of this boundary charge requires a redistribution of the ions: effectively negatively charged Sm'_{Ce} segregates to the space charge layer, while positively charged V_0 ⁻ accumulates at the grain boundaries. Therefore, it can be expected that the oxygen vacancies accumulates at the grain boundaries and the Sm'_{Ce} species segregates to the space charge layer. The above description has been theoretically proven by Guo [19].

As an oxygen vacancy crosses the grain boundary with positive potential core-layer sandwiched by the well-developed negatively charged space charged layer, it has a higher probability to be trapped to form an associate defect with Sm'_{Ce} . This will contribute to higher activation energy and thus higher true grain boundary resistivity. In the samples sintered at lower temperatures, the space charge layers are not well-developed and with less charge density. Note that higher temperature is needed to form a well-developed space charge layers. As an oxygen vacancy transports across the space charge layer, it will choose the path with less charge density of Sm'_{Ce} . Therefore, it has a lower probability to be trapped to form an associate defect with Sm'_{Ce} .

As described above and shown in Figs 1 and 2, the results of the grain size give strong evidence to support the mechanism of cation transport being the rate-limiting step in grain growth. Thus, upon various sintering temperatures, the Sm'_{Ce} mobility in $\text{Sm}_{0.2}\text{Ce}_{0.8}\text{O}_{1.9}$ can be the rate-limiting step of forming well-developed space charges layer. This further explains the above-described effect of sintering temperature on the resistivities.

4. Conclusion

In this work, near-completely soft-agglomerated $\text{Sm}_{0.2}\text{Ce}_{0.8}\text{O}_{1.9}$ powders have been prepared. The powders can yield 94% relative density by sintering at 1200[°]C for 20 hrs.

It was found that the sintering conditions of temperature and time have significant effects on the pellet resistivity. Sintering at the same temperature with longer time, the grain size increases and thus the apparent grain boundary resistivity decreases. By the measurements with the DC four-probe method, it was found that the overall resistivity of the polycrystalline $Sm_{0.2}Ce_{0.8}O_{1.9}$ material sintered at 1500◦C increases linearly with the reciprocal of the average grain size $(\frac{1}{d})$, and the grain resistivity can be obtained by extending the fitting line to $\frac{1}{d} = 0$.

The AC impedance spectroscopy has been used to distinguish the grain resistivity and the apparent grain boundary resistivity in a series of measurements on $\rm Sm_{0.2}Ce_{0.8}O_{1.9}$ ceramic electrolytes with various grain size distributions. The "brick layer" microstructural model has been used to provide an estimate of apparent grain boundary resistivity and to relate the electrical properties to the microstructural parameters. For samples sintered at 1500 °C, the relationship between the apparent grain boundary resistivity and the grain size corresponds well to the result via the DC measurement. For samples sintered at 1100–1200◦C, the true grain boundary resitivity was nearly two orders lower than that sintered at 1500◦C. This resistivity decrease is resulted from oxygen vacancy transport through not well-developed space charge layer, which has lower activation energy than the well-developed one.

It was also found that by lowering the sintering temperature to 1100–1200◦C, the overall resistivity decreases to about 31 ohm-cm at 700◦C measurement. This makes the $Sm_{0.2}Ce_{0.8}O_{1.9}$ material capable of working as SOFC's electrolyte at temperatures lower than 700° C to avoid possible reduction of cerium (4+).

Symbols

- *a* Pt electrode area $\text{(cm}^2\text{)}$
-
- C_g grain capacitance (F/cm²)
 C_{gb} grain boundary capacitance C_{gb} grain boundary capacitance (F/cm²)
 d grain size (*u*m)
- grain size (μm)
-
- $R_{\rm g}$ grain resistance (ohm)
 $R_{\rm g}$ grain boundary resistan grain boundary resistance (ohm)
- *t* pellet thickness (cm)
- *V*·· $V_0^{\text{...}}$ oxygen vacancy
 δ_{gb} grain boundary t
- grain boundary thickness (μm)
- λ dimensionless geometrical factor
- σ conductivity (S/cm)
- ρ overall resistivity (ohm-cm)
- ρ' electrical resistivity (ohm-cm)
- $\rho_{\rm g}$ grain resistivity (ohm-cm)
- ρ_{gb} true grain boundary resistivity (ohm-cm)
- $\frac{\delta}{d} \rho_{\rm gl}^*$ apparent grain boundary resistivity (defined as ρ_{gb}) (ohm-cm)
- ε_g relative grain dielectric permittivity (C²/N-cm²)
- ε_{gb} relative grain boundary dielectric permittivity $(C^2/N-cm^2)$

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